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PATENT APPLICATION

ORIGINAL

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IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Sompong P. OLARIG et al. **Confirmation No.:** 7601

Application No.: 09/735,267 **Examiner:** P. R. Myers

Filing Date: 12/12/2000 **Group Art Unit:** 2112

Title: SYSTEM SUPPORTING MULTICAST MASTER CYCLES BETWEEN DIFFERENT BUSSES IN A COMPUTER SYSTEM

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith in **triplicate** is the Appeal Brief in this application with respect to the Notice of Appeal filed on **03/18/2004**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $330.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$110.00
( )	two months	$420.00
( )	three months	$950.00
( )	four months	$1480.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$330.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

(X) I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit: **04/19/2004**

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Respectfully submitted,

Sompong P. OLARIG et al.

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ORIGINAL

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Sompong P. OLARIG et al.	Confirmation No.:	7601
Serial No.:	09/735,267	Group Art Unit:	2112
Filed:	12/12/2000	Examiner:	P. R. Myers
For:	System Supporting Multicast Master Cycles Between Different Busses In A Computer System	Docket No.:	200304316-1

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Date: April 19, 2004

Sir:

Appellant hereby submits this Appeal Brief in connection with the above-identified application. A Notice of Appeal was filed on March 18, 2004.

I. REAL PARTY IN INTEREST

The real party in interest is the Hewlett-Packard Company through its merger with Compaq Computer Corporation which owned Compaq Information Technologies Group, L.P. (CITG).

II. RELATED APPEALS AND INTERFERENCES

Appellant is unaware of any related appeals or interferences.

III. STATUS OF THE CLAIMS

Originally filed claims:	1-24.
Claim cancellations:	None.
Added claims:	None.
Presently pending claims:	1-24.
Presently appealed claims:	1-24.

IV. STATUS OF THE AMENDMENTS

No claims were amended after the Final Office Action dated February 17, 2004.

V. SUMMARY

Computers typically comprise one or more buses which permit communication of data between various components of the computer. See Disclosure, page 2, lines 8-9. In accordance with at least some bus protocols, a device coupled to a bus may function as a "master" to initiate a transaction over the bus to a "slave" device. The master-slave relationship helps to ensure a coordinated usage of the bus by multiple devices. In a typical bus transaction, a bus master may send information, including address, data and control information, to a target device operating as a slave during that bus transaction. In certain situations, however, it may be desirable to broadcast the information to multiple targets. For example, in a fault-tolerant environment it is desirable to perform fast backup of data such as may be possible using mirrored disk drives. Disclosure, page 5, lines 4-9.

Applicants' contribution relates to improving the efficiency of broadcast transactions. Applicants' contribution generally relates to broadcasting data to multiple target devices during a single bus transaction. Disclosure page 6, lines 4-5. In accordance with at least one embodiment of Applicants' invention, data may be broadcast from one bus to another via a bus bridge. Applicants' Figure 4 illustrates an exemplary embodiment. As shown, bridge 450 interconnects first and second peripheral component interconnect (PCI) buses 425 and 475. Devices on both buses 425, 475 may communicate with each other via bridge 450. Figure 4 also shows first and second multicast buses 460 and 465 that couple to the bridge 450 as shown. Sideband signals 430 and 480 are also included between the bus devices and the bridge 450. Disclosure page 12, line 23 through page 13, line 14.

The system depicted in Figure 4 supports multicast and non-multicast cycles through the bridge 450 in an efficient manner. By way of an example, device 435 on PCI bus 425 may function as a master to transmit a broadcast message intended for multiple targets on PCI bus 475. Using Applicants' protocol, the master device 435 initiates a master cycle on bus 425 targeting the bridge 450. Master device 435 also transmits control and data signals on

multicast bus 460 identifying the start and type of multicast cycle and the intended targets. Disclosure page 13, lines 15-23. Data is communicated through the bridge 450 between buses 425 and 475 while multicast information is transmitted over multicast buses 460 and 465. The sideband signals 430, 480 are used to indicate to the bridge 450 whether the transaction is a multicast cycle and, if so, the identity of the multiple targets. This information is used by the bridge and target devices to correctly decode the transmission on the buses 425 and 475. The table on page 14 illustrates one embodiment of how four data signals on the multicast buses can be encoded to identify the target(s) of a multicast cycle that is transmitted over the PCI buses 425 and 475. For example, "the data signals are capable of signaling individual targets on a bus, various combinations of devices as targets, all devices on bus 425 as a target, all devices on bus 475 as a target, and all devices on both busses as a target." Page 15, lines 11-14.

Claims 1 and 16 are exemplary of various embodiments of the invention and are as follows:

1. A computer system, comprising:
   a first computer bus connected to a first plurality of bus devices;
   a second computer bus connected to a second plurality of bus devices;
   a bridge coupling together said first computer bus and said second computer bus;
   a first multicast bus connecting to said first plurality of bus devices and a second multicast bus connecting to said second plurality of bus devices;
   wherein one of the first plurality of bus devices is capable of transmitting a multicast signal to at least two of said second plurality of bus devices, which are identified by a signal transmitted on said first multicast bus and said second multicast bus.

16. A method of transmitting a multicast signal between a device on a first bus to multiple targets on a second bus, and wherein the first bus and the second bus are coupled together by at least one bus bridge, comprising the acts of:

generating data on the first bus that is intended for multiple targets on the second bus;

identifying the multiple targets on the second bus via a target identification signal transmitted on a first and second multicast bus; and

signaling the bridge that a multicast cycle has been initiated on the first bus;

relaying the data on the first bus to the second bus by the bridge;

indicating that data for a multicast cycle is appearing on the second bus; and

capturing the multicast data at the targets identified by the target identification signal.

VI. ISSUE(S)

(1) Whether claims 1 and 13 are patentable under 35 U.S.C. § 103 over Ananthan (U.S. Pat. No. 5,634,138) in view of Gehman (U.S. Pat. No. 6,260,093);

(2) Whether claims 2-7, 14 and 16-21 are patentable under 35 U.S.C. § 103 over Ananthan in view of Gehman and McMinn (U.S. Pat. No. 6,097,403);

(3) Whether claims 8-12, 15, and 22-24 are patentable under 35 U.S.C. § 103 over Ananthan in view of Gehman, McMinn and "PCI System Architecture.

VII. GROUPING OF CLAIMS

For purposes of this appeal, Applicants have selected claim 1 from the first group and claim 16 from the second group. The third group (claims 8-12, 15, and 22-24) comprise dependent claims that depend from either claims 1 or 16. For purposes of this appeal, Applicants will let the third group of claims stand or fall with their associated independent claims.

In the second group, claims 2-7 and 14 depend from claim 1, not independent claim 16. Applicants do not necessarily consider claim 16 to be representative of any of claims 2-7 and 14. Although grouped together, Applicants do not argue any of claims 2-7 and 14 separate from claim 16. Claims 2-7 and 14 are patentable at least for the same reason as claim 1.

VIII. ARGUMENT

A. The Ananthan Reference

Ananthan is directed to burst broadcasting on a PCI bus. Figure 1 of Ananthan provides a system drawing that is labeled as "prior art" that shows various devices coupled to a PCI bus 30. Figure 2 reflects Ananthan's contribution and illustrates one device 60 and three devices 70 coupled to a bus 50. As shown, device 60 can broadcast data to multiple devices 70 all on the same bus. See also col. 3, lines 25-31. Such broadcast transactions are not described as passing through bridge 57 or otherwise being transmitted to devices on other buses. In passing, Ananthan notes that the multicasting principles employed on bus 50 (Figure 2) could be employed at any tier of buses shown in Figure 1, for example bus 30 or bus 35. Moreover, Ananthan fairly discloses multicast transmissions between devices on the same bus and such multicast bus could be implemented at various tiers of a computer system. Ananthan does not disclose or even suggest that devices on one bus could initiate multicast transactions to devices on another bus or that the coordinated action of two different buses are needed to effectuate a multicast cycle.

B. The Gehman Reference

Gehman is directed to arbitrating access to multiple busses in a data processing system. Figure 2 of Gehman shows two busses 202 and 204 interconnected by a bridge 206. Devices on one of the busses can initiate transactions to devices on the other bus. Gehman does not teach or suggest multicast bus transactions.

C. The McMinn Reference

McMinn appears only relevant for its teaching of the use of "sideband signals apart from standard bus signals. As will become clear below, the Examiner's rejections are in error for reasons generally unrelated to the teachings of McMinn and thus a more in depth explanation of McMinn is not necessary.

D. The PCI System Architecture Reference

This reference appears only relevant for its teaching of the use of multiple PCI bridges. As will become clear below, the Examiner's rejections are in error

for reasons generally unrelated to the teachings of the PCI System Architecture reference and thus a more in depth explanation of this reference is not necessary.

1. Claim 1

Claim 1 requires, among other features, a system to have "a first computer bus," "a second computer bus," "a first multicast bus," "a second multicast bus," and "a bridge"—configured as described in the claim. The claimed first and second computer busses couple to the bridge. Further, a first plurality of devices connects to the first multicast bus and a second plurality of devices connects to the second multicast bus. Claim 1 also requires that "one of the first plurality of bus devices is capable of transmitting a multicast signal to at least two of said second plurality of bus devices, which are identified by a signal transmitted on said first multicast bus and said second multicast bus."

The Examiner's argument is summarized below:

- While the art of record does not show four buses as referenced in claim 1, a prior art bus can, in fact, be two buses. Thus, two buses in the art of record can suffice for the four claimed buses.
- Ananthan teaches multicasting between devices connected to the same bus.
- Gehman discloses a bridge.
- Thus, the combination of Ananthan and Gehman collectively render obvious the notion of multicasting through a bridge.

Applicants respectfully submit that the Examiner's rejection of claim 1 is flawed for multiple reasons. On pages 5-6 of the Final Office Action, the Examiner identified bus 30 of Ananthan's Figure 1 as being both the claimed first computer bus and the claimed first multicast bus. The Examiner also identified Ananthan's bus 50 shown in Figure 2 as being both the second computer bus and the second multicast bus. The Examiner stated that "[t]here is no requirement that the first computer bus and the first multicast bus be separate busses." Final Office Action page 2. On page 2, the Examiner supported this conclusion that the claimed computer bus and the claimed multicast bus could be

one and the same bus by analogizing the claim to "a multiplexed address/data bus [that] is both an address bus and a data bus."

The Examiner erred in concluding that one bus in the art can be both a claimed computer bus and a claimed multicast bus. Each of the four buses listed in claim 1 is referred to as a "bus" with a different preceding descriptor to differentiate one bus from another (i.e., "a first computer bus," "a second computer bus," "a first multicast bus," "a second multicast bus"). If two of the claimed buses could be implemented as a single bus, then there would be no reason to use two different names for what is the same item. Applicants respectfully submit that the Examiner's reading of claim 1 is disingenuous with regard to the plain language of the claims and when read against Applicants' disclosure which shows and describes the operation of four separate buses. Further, the Examiner's reference to a multiplexed address/data bus being both an address bus and a data bus is incorrect. A multiplexed bus is one bus that has separate address phases and data phases that are multiplexed in time, and thus is not two buses implemented as a single bus. For at least this reason, the Examiner erred in rejecting claim 1.

The Examiner correctly concluded that Ananthan does not teach a multicast master being on a different bus than the targets. Office Action page 2. Instead, the Examiner turned to Gehman that, according to the Examiner, teaches "how a master on a first bus can gain access to a target on a second bus by translating the signals across a bus bridge." Office Action page 2. The Examiner concluded that "[i]t would have been obvious to a person of ordinary skill in the art at the time of the invention to allow the master to be on a different bus because this would have allowed greater system flexibility." The Examiner failed to properly justify combining Ananthan and Gehman in the obviousness rejection. Specifically, the Examiner did not explain how permitting the master to be on a different bus than the targets would have been suggested by the art nor how that configuration would have enabled "greater system flexibility."

In the Final Office Action, the Examiner attempted to address this issue. "In regards to applicants argument that the examiner has not established how

achieving greater flexibility constitutes a sufficient ground to combine references in an obviousness analysis: 'The normal desire of scientists or artisans to improve upon what is already generally known provides the motivation.'" Final Office Action page 4 (quoting *In re Peterson*, 315 F.3d 1325, 1330 (Fed. Cir. 2003)). Applicants respectfully submit that the Examiner has misread and misapplied the *Peterson* case. Peterson's claimed invention included a range that fell within a broader range disclosed in the prior art. *In re Peterson*, 315 F.3d 1325, 1327, 1328 (Fed. Cir. 2003) (the claim required "about 1 to 3 percent rhenium" and the prior art disclosed 0 to 7 percent rhenium). The Federal Circuit held that the Board did not err in rejecting the claims as obvious. "The motivation" referred to in the sentence quoted above by the Examiner in the present application referred to the motivation to determine where in a disclosed range the optimum range lies. The Examiner did not quote the entire sentence which reads as follows: "The normal desire of scientists or artisans to improve upon what is already generally known provides the motivation ***to determine where in a disclosed set of percentage ranges is the optimum combination of percentages***." *Id.* at 1330 (emphasis added). Moreover, in contrast to the present application, motivation to combine prior art in an obviousness analysis was not an issue in *Peterson*. The Examiner unfortunately has presented a statement from *Peterson* out of context with regard to the present application.

Even if greater flexibility were to result from modifying Ananthan in light of Gehman as suggested by the Examiner, the Examiner's reasoning still fails to justify combining Ananthan and Gehman. That is, the Examiner has not established how achieving greater flexibility constitutes a sufficient ground to combine references in an obviousness analysis. Surely if heightened flexibility was enough to permit prior art references to be combined together, then virtually all references could be combined together—one could almost always conjure up some form of heightened flexibility from a combination of references. Such a result clearly is not intended under our patent system. Moreover, Applicants respectfully submit that the Examiner has improperly glossed over a crucial

element of an obviousness analysis. As the Federal Circuit made abundantly clear:

> Measuring a claimed invention against the standard established by section 103 requires the oft-difficult but critical step of casting the mind back to the time of invention, to consider the thinking of one of ordinary skill in the art, guided only by the prior art references and the then-accepted wisdom in the field. Close adherence to this methodology is especially important in the case of less technologically complex inventions, where the very easy with which the invention can be understood may prompt one "to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher." Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references."

In re Dembiczak, 175 F.3d 994, 999 (Fed. Cir. 1999) (citations omitted) (reversing the examiner's rejection for lack of a proper showing to support combining prior art references). The Examiner has improperly used hindsight to compare the claims against the art of record. Gehman is not related to multicast transactions and the Examiner has not offered a legally permissible reason as to why one of ordinary skill in the art would have been motivated by the prior art to use the teachings of Gehman with Ananthan in the manner suggested by the Examiner. Ananthan does not suggest that it would be desirable to conduct multicast transactions between busses through a bridge and thus there is no suggestion or motivation for modifying Ananthan to include trans-bridge multicasting.

On pages 4-5 of the Final Office Action, the Examiner appears to conclude that combining the bridge teaching of Gehman with the single bus multicast transaction of Ananthan would have been obvious because using bridges to permit devices on different buses to communicate with each other is well known. "In this case without any hindsight anyone of any skill in the art would have recognized using a bus bridge to access devices on another bus would have been obvious (Especially since this is the purpose of bus bridges)." The Federal Circuit has cautioned against

such conclusions. "35 U.S.C. § 103 requires that obviousness be determined with respect to the invention as a whole. This is essential for combination inventions, for generally all combinations are of known elements." *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143 (Fed. Cir. 1985). Thus, while bridges are indeed well known for coupling together multiple buses, it was not known to use a bridge as Applicants have claimed—to support multicast transactions through a bridge.

For any or all of the reasons stated above, the Examiner erred in rejecting claim 1. Claims 2-15 depend on or from claim 1 and thus are patentable at least for the same reason as claim 1.

2. Claim 16

The Examiner rejected method claim 16 as obvious over the combination of Ananthan, Gehman, and McMinn. The Examiner erred in rejecting claim 16 for several reasons. First, claim 16 requires at least six "acts" and the Examiner has not addressed all of the claimed acts. For instance, the Examiner has not established where in the art of record the acts of "signaling the bridge that a multicast cycle has been initiated," "indicating that data for a multicast cycle is appearing on the second bus," and "capturing the multicast data at the targets identified by the target identification signal" can be found. Applicants contend that the art of record is devoid of any such specific teachings and thus the Examiner failed to establish a *prima facie* case of obviousness with regard to claim 16.

Further, the Examiner has not adequately established where in the art of record the act of "identifying the multiple targets on the second bus via a target identification signal transmitted on a first and second multicast bus" is found. For this limitation, the Examiner noted that Ananthan discloses, in the words of the Examiner, "identifying multiple targets on a bus via a target identification signal transmitted on the bus"—which all occurs on the same bus in Ananthan. The claim limitation quoted above,

however, requires identifying targets on a separate bus from the bus on which the target identification signal is transmitted.

Additionally, claim 16 refers to four buses—first and second buses and first and second multicast buses. As explained above, the Examiner's attempt to read a single bus in the art as being two buses is disingenuous and simply incorrect.

Claim 16 requires "generating data on the first bus that is intended for multiple targets on the second bus" and "identifying the multiple targets on the second bus via a target identification signal transmitted on a first and second multicast bus." Thus, the first and second buses are used for the communication of data in a multicast cycle, while the multicast buses are used to identify the targets of the multicast cycle. None of the art of record teaches or even suggests such a coordinated action of different buses.

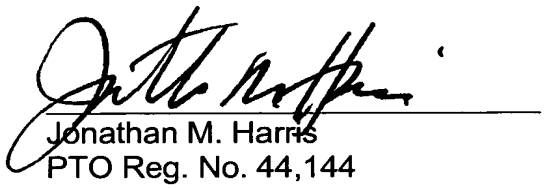
The Examiner used McMinn in the rejection of claim 16 for its teaching of "sideband signals" although claim 16 does not explicitly refer to sideband signals. The Examiner concluded that it would have been obvious to combine McMinn with Ananthan and Gehman because "this would have allowed for faster multicast setup by eliminating the setup cycle." Office Action page 3. At the risk of being redundant, Applicants respectfully submit that merely noting a benefit that might result from a combination of references is not sufficient to support a rejection of a claim based on a hypothetical and speculative combination. The prior art (not the claim) must suggest the desirability of making the combination. *See In re Fine*, 837 F.2d 1071, 1075 (Fed. Cir. 1988) (reversing examiner's rejection).

For any or all of these reasons, the Examiner erred in rejecting claim 16. Claims 17-24 depend on or from claim 16 and thus are patentable at least for the same reason as claim 16.

IX. CONCLUSION

For the reasons stated above, Applicants respectfully submit that the Examiner erred in rejecting all pending claims. If any fees or time extensions are inadvertently omitted or if any fees have been overpaid, please appropriately charge or credit those fees to Hewlett-Packard Company Deposit Account Number 08-2025 and enter any time extension(s) necessary to prevent this case from being abandoned.

Respectfully submitted,



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APPENDIX TO APPEAL BRIEF

CURRENT CLAIMS

1. (Original) A computer system, comprising:

a first computer bus connected to a first plurality of bus devices;

a second computer bus connected to a second plurality of bus devices;

a bridge coupling together said first computer bus and said second computer bus;

a first multicast bus connecting to said first plurality of bus devices and a second multicast bus connecting to said second plurality of bus devices;

wherein one of the first plurality of bus devices is capable of transmitting a multicast signal to at least two of said second plurality of bus devices, which are identified by a signal transmitted on said first multicast bus and said second multicast bus.

2. (Original) The system of claim 1, wherein the first plurality of bus devices are capable of transmitting a sideband signal to said bridge indicating a multicast cycle.

3. (Original) The system of claim 2, wherein the bridge relays the multicast cycle to said second computer bus in response to receipt of the sideband signal.

4. (Original) The system of claim 3, wherein said at least two of said secondary plurality of bus devices that are identified by a signal transmitted on the first and second multicast busses, each receive and decode the multicast cycle relayed by said bridge.

5. (Original) The system of claim 4, wherein said bridge also transmits a sideband signal to said second plurality of bus devices substantially simultaneously with relaying the multicast cycle.

6. (Original) The system of claim 5, wherein said first computer bus and said second computer bus comprise a PCI bus and said bridge comprises a PCI-to-PCI bridge.

7. (Original) The system of claim 2, wherein said bridge comprises a PCI-to-host bridge that connects to a host bus.

8. (Original) The system of claim 7, wherein said second computer bus comprises a second PCI bus, and a second PCI-to-host bridge couples said host bus to said second PCI bus.

9. (Original) The system of claim 8, wherein the first PCI-to-host bridge transmits a sideband signal to said second PCI-to-host bridge indicating a multicast cycle originating on said first PCI bus.

10. (Original) The system of claim 9, wherein in response to the sideband signal from said first PCI-to-host bridge, said second PCI-to-host bridge captures data transmitted on said host bus from said first PCI-to-host bridge.

11. (Original) The system of claim 10, wherein the second PCI-to-host bridge relays the data captured from the host bus onto the second PCI bus, and wherein said at least two of said secondary plurality of bus devices that are identified by a signal transmitted on the first and second multicast busses, each receive and decode the multicast cycle relayed by said second PCI-to-host bridge.

12. (Original) The system of claim 11, wherein said second PCI-to-host bridge also transmits a sideband signal to said second plurality of bus devices substantially simultaneously with relaying the multicast cycle.

13. (Original) The system of claim 1, wherein one of the second plurality of bus devices is capable of transmitting a multicast signal to at least two of said first

plurality of bus devices, which are identified by a signal transmitted on said first and second multicast busses.

14. (Original) The system of claim 3, wherein the sideband signals are transmitted on the multicast busses.

15. (Original) The system of claim 12, wherein the sideband signals are transmitted on the multicast busses.

16. (Original) A method of transmitting a multicast signal between a device on a first bus to multiple targets on a second bus, and wherein the first bus and the second bus are coupled together by at least one bus bridge, comprising the acts of:

generating data on the first bus that is intended for multiple targets on the second bus;

identifying the multiple targets on the second bus via a target identification signal transmitted on a first and second multicast bus; and

signaling the bridge that a multicast cycle has been initiated on the first bus;

relaying the data on the first bus to the second bus by the bridge;

indicating that data for a multicast cycle is appearing on the second bus; and

capturing the multicast data at the targets identified by the target identification signal.

17. (Original) The method of claim 16, wherein the act of generating data on the first bus includes transmitting data on the first bus according to the protocol of the first bus.

18. (Original) The method of claim 16, wherein the act of signaling the bridge occurs via a sideband signal between the device generating the data and the bridge.

19. (Original) The method of claim 16, wherein the act of indicating the data for a multicast cycle is appearing on the second bridge occurs via a sideband signal between the bridge and devices resident on the second bus.

20. (Original) The system of claim 16, wherein the first bus and the second bus comprise PCI busses.

21. (Original) The system of claim 20, wherein the bridge comprises a PCI-to-PCI bridge.

22. (Original) The system of claim 20, wherein two bridges couple the PCI busses together.

23. (Original) The system of claim 22, wherein the two bridges are connected to a host bus.

24. (Original) The system of claim 23, wherein the two bridges comprise PCI-to-host bridges.